Mingkai Miao

+86 15108472550
mmiao815@connect.hkust-gz.edu.cn
https://github.com/tracymiao111
https://www.linkedin.com/in/mingkai-miao-5460b1289

Education

Hong Kong University of Science and Technology (Guangzhou) Aug. 2024 – Present
the 2nd year PhD student in Microelectronics Thrust

- Supervised by **Prof. Hongce Zhang**
- GPA: 4.19/4.3

University of Illinois at Urbana-Champaign Jan. 2023 – May. 2024
Master student in Electrical and Computer Engineering

- GPA: 3.91/4.0
- Courses taken: Analog Circuit Design, IoT and Cognitive Computing, Computer Organization and Design, Computer Organization, System-On-Chip Design, Embedded System Verification, Parallel Computer Architecture.

University of Electronic Science and Technology of China Sep. 2017 – Sep. 2021
B.Eng. in Electronic and Information Engineering

- Engineering GPA: 3.898/4.0 for 77-credit
- Mathematics GPA: 4.0/4.0 for 18.5-credit
- Ranking top 20% with CGPA 3.72/4.0

Selected Publication

Conference:

LeGend: A Data-Driven Framework for Lemma Generation in Hardware Model Checking 2026
Mingkai Miao, *Guangyu Hu, Wei Zhang, Hongce Zhang* DAC

BDD2Seq: Enabling Scalable Reversible-Circuit Synthesis via Graph-to-Sequence Learning 2026
Mingkai Miao, *Jianheng Tang, Guangyu Hu and Hongce Zhang* AAAI (Oral)

FORWORD: Accelerating Formal Datapath Verification via Word-Level Sweeping 2026
Ziyi Yang, Guangyu Hu, Xiaofeng Zhou, ***Mingkai Miao****, Changyuan Yu, Wei Zhang and Hongce Zhang* DATE

Primary Project

Three Research Projects on AI for Hardware Model Checking Mar 2025 – Present
Hong Kong University of Science and Technology, Guangzhou Guangzhou & HK, China

- Two of them are submitted and wait for review; one is in flight.

BDD Variable Reordering Using Graph to Sequence Learning Sep 2024 – Apr 2025
Hong Kong University of Science and Technology, Guangzhou Guangzhou, China

- Utilize Graph Encoder with Pointer Network Decoder & Beam Search to explore promising BDDs variable ordering sequences.
- Further applied in BDD-based reversible circuit synthesis and achieve great performance on Quantum Cost saving and computation acceleration.

FPGA-Optimized Parallelism in Deep Neural Networks Jan 2024 – May 2024
University of Illinois at Urbana-Champaign Champaign, US

- Implement the LeNet network for handwriting recognition tasks on the Xilinx Pynq Z2 Board from three aspects: Hardware, Model Architecture, and Software. In terms of Hardware, use High Level Synthesis to design the hardware accelerator. For Model Architecture, optimize using Pruning and Quantization. On the Software side, an Interrupt Handler is designed to achieve Function Level Parallelism (with Dataflow support at the Hardware level). Compared to the CPU platform on Pynq Z2, a final acceleration of **63.7x** is achieved.
- **Project Link:** https://github.com/tracymiao111/CS533-FinalProject

5 stage pipelining RISC-V processor design Aug 2023 – Dec 2023
University of Illinois at Urbana-Champaign Champaign, US

- Implemented the multicycle 5 stage pipelined RV32I processor
- Implemented one-cycle hit i-cache, L2 unified cache and fully parameterized mutli-level d-caches (PLRU replacement policy) with an eviction buffer
- Implemented RISC-V M Extension, simple hardware prefetching
- Achieved the **3rd place (33 groups)** in UIUC ECE411 Computer Organization and Design RV32I Competition in December
- **Project Link:** https://github.com/tracymiao111/Pipelined-CPU-Design

Low dropout regulator design Apr 2023 – May 2023
University of Illinois at Urbana-Champaign Champaign, US

- Designed a low dropout regulator (LDO) used to generate supply voltage to sensitive analog circuits on Cadence Virtuoso
- Achieved specifications including Input/Output voltage, Load current, DC load/line regulation, etc
- **Project Link:** https://github.com/tracymiao111/LDO-Design

Honors and Awards

Winner of University's First-class Merit-based Scholarship Fall 2018 & 2019
University of Electronic Science and Technology of China

Postgraduate Studentship Full Scholarship(PGS) Sep 2024 - Present
Hong Kong University of Science and Technology

Service

Artifact Evaluation Committee
TACAS 2025, TACAS 2026

Program Committee
AAAI 2026

Sub-Reviewer
DAC 2026

Skills

Languages: English (IELTS 7.0; GRE 329), Chinese (Native)
Programming: SystemVerilog, C++, Python
Document Creation: Latex, Markdown